METHODS AND APPARATUSES FOR PROVIDING SYNCHRONIZATION IN A COMMUNICATION NETWORK

Field of Invention

The present invention refers to methods and apparatuses for providing synchronization in communication networks wherein data are transferred on bitstreams that are divided into recurrent frames.

Technical Background and Prior Art

Today, new types of communication networks are being developed for the transfer of information using circuit-switched channels established on time division multiplexed bitstreams, wherein each bitstream is divided into regularly recurrent frames, or cycles, each frame in turn typically being divided into time slots.

An example of such a network is the DTM (Dynamic synchronous Transfer Mode) network, which for example is described in "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994.

On each bitstream in such a network, a head-end node arranged at an uppermost upstream location on the bitstream is provided to write, i.e. transmit, a regularly recurrent frame synchronization signal into one or more time slots on the bit-stream, thereby defining frames of said bitstream and thus establishing frame synchronization for downstream located nodes to synchronize their operations to.

When forming a network comprising several links or bitstreams, these are connected using so called switch nodes. When transferring synchronous or isochronous communication in a TDM fashion, the frame rate of the different network bitstreams need to be synchronized in order to avoid problems such as loss of data (also known in the art as "slip").

This is generally provided by a synchronization scheme that ensures the same frame repetition frequency on all communication bitstreams in the network. Such a synchronization arrangement may for example be a hierarchical synchronization structure of the kind described in EP 522 607 A1, wherein frame synchronization is propagated from one single master clock node to all downstream nodes in a tree-like fashion using the network as such for propagating the frame synchronization signal.

A disadvantage with such prior art schemes is that they allow little freedom as to the construction, build up and configuration of the network, requiring the use of a very strict, top-down hierarchy. Also, limitations as to network management during link failures, re-establishment of link synchronization, and the like, apply correspondingly.

An object of the invention is therefore to provide simple scheme for achieving network synchronization which allows greater freedom as to the construction, build up and configuration of the network, as well as to network management during link failures, re-establishment of link synchronization, and the like.

Summary of the invention

The above mentioned and other objects of the invention are achieved by the invention as defined in the accompanying claims.

According to an aspect of the invention, a recurrent frame synchronization signal on a bitstream of said network is detected at a node of the network. Information relating to the frame synchronization situation caused by the detected recurrent frame synchronization signal is then generated. This information is then transmitted to a frame synchronization providing node of said network, said information preferably being used at said frame synchronization providing node for affecting the provi-

sion of said recurrent frame synchronization signal based thereupon.

Hence, the invention provides for a node connected to a bitstream of the network to send feedback information related to the frame synchronization situation, typically at the location of the node, to a frame synchronization providing node that controls, directly or indirectly (via one or more intermediate nodes), the provision of frame synchronization on said bitstream. Typically, said frame synchronization providing node will be a so-called head-end node of a bitstream.

Vice versa, the invention provides for a node, which is arranged to establish frame synchronization on a bitstream by transmitting frame synchronization information thereto, to control the establishment of frame synchronization on said bitstream, either directly or indirectly (via an intermediate trigger node), based upon frame synchronization information provided by, or via, one or more nodes typically connected to said network at a location downstream with respect to said trigger node.

In fact, if desired, a node connected to a bitstream at a location downstream with respect to the frame synchronization providing node, such as a head-end node, may be arranged to actually control the frame rate on said bitstream by repeatedly instructing the head-end node, in a master-slave type of relationship, on how or when to provide the frame synchronization signal.

An advantage of the invention is that it allows for greater freedom when designing the network configuration by providing a mechanism which advantageously makes it possible to circumvent or at least lighten the prior art requirement of a strict hierarchical top-down synchronization control and distribution scheme.

According to a preferred embodiment of the invention, as taken in the context of a switch node arranged to switch time slot data between a first bitstream and a second bitstream of said network, a frame drift between

said first and said second bitstream is determined, wherein the features of said frame drift is used to define said information relating to the frame synchronization established by said recurrent frame synchronization information. This information is then preferably used at the frame synchronization providing node for controlling the transmission of said recurrent frame synchronization information based thereupon with the aim of eliminating said frame drift.

Consequently, the invention very advantageously makes it possibly to interconnect two or more network sections, wherein each network section has its frame synchronization provided by its own head-end node, said head-end nodes being independent of each other either because it has been so configured at network set-up, or as a result of a link of node failure that has eliminated a previously prevailing master-slave relationship between the two.

In prior art, this would not be possible, since frame synchronization were required to be distributed in a hierarchical top-down tree like fashion in order to ensure synchronization consistency throughout the network. The use of two independent head-end nodes would inevitably lead to frame drift between different parts of the network, consequently causing data slip or data congestion, since it is practically impossible to provide to master nodes operating at the exact same bit rate and frame frequency.

However, according to the invention, by continuously informing one or both of the frame synchronization head-end nodes of the frame drift situation, preferably taken at the point where the two networks sections are interconnected, this information may then be used to continuously adjust the frame frequency established by the master nodes so that any frame drift tendency is continuously eliminated.

As is understood, this aspect of the invention in a fundamental way provides for greater freedom as to the construction, build up and configuration of the network, as well as to network management during link failures, re-establishment of link synchronization, and the like.

Preferably, said information relating to the frame synchronization situation are transmitted to said at least one frame synchronization providing node of said network using one or more time slots of one or more bitstreams of said network. Although an alternative wherein a communication system being external to said network may also be used to transmit said data, the alternative of using the network itself for this transmission provides a simple and preferred channel of communication.

Furthermore, the controlling of the transmission of said recurrent frame synchronization information preferably comprises controlling the size of one or more frames of a bitstream of said network. Also, the size of one or more frames is preferably controlled by adjusting the number of slots or bits provided within one or more frames, for example the number of fill slots, also called guard band slots, provided to said one of more frames. According to another alternative, the frame size could also be controlled by controlling the bit rate used within said one or more frames, for example by controlling a bit clock or counter used at the synchronization providing node.

As is understood, said data, typically when relating to the frame drift between two bitstreams, may also be used to inform a head-end node of one of the bitstreams in case of a link failure, or the like, with respect to the other bitstream.

Also, as understood by those skilled in the art, the features of the invention are readily realized using conventional electronic circuitry and/or network software tools.

Furthermore, the invention is advantageously used in DTM networks. In DTM, the requirements on network synchronization are such that an input and an output bitstream may be arbitrarily located in phase with respect to each other as long as there is no persistent phase drift between the two. Furthermore, frame synchronization is provided in a tree-like, top-down manner. In DTM, the time slots of each frame are furthermore divided into two groups, control slots and data slots, and wherein each node typically has access to at least one control slot and a number of data slots within each frame, said number of data slots being dynamically adjustable based upon the bandwidth requested by the end users being served by the respective node. The frame synchronization signal is then typically transmitted as such a time slot to mark the start of each frame.

It is to be noted that said recurrent frame synchronization signal may be provided in many different forms. For example, in the preferred embodiment, as will be described in detail below with reference to the drawings, the recurrent frame synchronization signal is provided in the form of a regularly recurring frame synchronization time slot, said time slot as such, i.e. by its mere location in the bitstream, defining each frame of a bitstream, for example by being located at the start of each frame. However, in another embodiment, said recurrent frame synchronization information does not need to define the frame location by the its mere location in the bitstream. Instead, its the content or "message" of the information that provides data as to the timing of one or more frames of the bitstream, for example providing data as to where (or rather when) each of the next ten frames starts and/or ends.

Further aspects, advantages, and features of the invention will be more fully understood from the following detailed description of exemplifying embodiments thereof.

Brief Description of the Drawings

Exemplifying embodiments of the invention will now be described with reference to the accompanying drawings, wherein:

Figs. 1-4 schematically show bitstreams of a communication network operating according to embodiments of the invention;

Fig. 5 schematically shows the configuration of a bitstream of the kind shown in Figs. 1 to 4;

Figs. 6a and 6b schematically illustrate frame synchronization situations with respect to a first and a second bitstream; and

Fig. 7 schematically shows a network node according to an embodiment of the invention.

Detailed Description of Preferred Embodiments

The configuration of a simple network 10a operating according to an embodiment of the invention will now be described with reference to Fig. 1. The network 10a in Fig. 1 comprises two separate bitstreams B1 and B2 propagating in the directions indicated by arrows in Fig. 1 and hence transferring data in opposite directions between nodes 12-18 of the network. The nodes typically provide network access to end users connected to the respective node.

On bitstream B1, the uppermost provided node 12 is head-end node and is thus arranged to define frame synchronization by transmitting a regularly recurrent frame synchronization signal, referred to below as frame start signal, and a regularly recurrent guard pattern on bitstream B1, indicating the start and end, respectively, of each frame, as is described more in detail below with reference to Fig. 5.

Similarly, on bitstream B2, the uppermost provided node 18 is head-end node and is thus arranged to provide

frame synchronization by transmitting corresponding frame start signals and guard patterns on bitstream B2.

In this embodiment, it is assumed that node 12 acts as a so-called synchronization master node, referred to below as "master node", whereas the node 18 acts as a so-called synchronization slave node, referred to below as "slave node". In this context, this means that node 18 will transmit its frame start signal on bitstream B2 in synchronization with the received frame start signal provided by the master node 12 on bitstream B1.

The intermediate nodes 14 and 16 are arranged to synchronizes their bitstream access operations according to the frame start signal provided on bitstream B1 when transmitting data to or receiving data from bitstream B1, and according to the frame start signal provided on bitstream B2 when transmitting data to or receiving data from bitstream B2.

In the embodiment shown in Fig. 1, and according to the invention, it is assumed that node 16 is arranged to use, e.g., one time slot per frame on bitstream B2 to transmit information, relating to the timing of the reception of the frame start signal on bitstream B1, to the master node 12. This information is then received by the master node 12 and used at the master node 12 as a basis for determining how to control the provision of the frame start signal on bitstream B1. If, for example, the information provided by node 16 suggests that it would be desirable to lower the network frame rate, the master node 12 may decide to increase the number of time slots included in the guard band in each frame on bitstream B1, thereby increasing the length of each frame on bitstream B1 (and consequently on bitstream B2 due to the master slave relationship between the master node 12 and the slave node 18). There may be many different reasons for node 16 to suggest an increase or decrease in the frame rate. For example, data congestion in the operation of the end users served by the node 16, or rate changes in

another network also connected to the node 16. In fact, if desired, the node 16 may act as the "true" master node of the network, repeatedly instructing the master node 12 on how to increase or decrease the bitstream frame rate.

The configuration of another network 10b operating according to the invention will now be described with reference to Fig. 2. The network 10b is an expansion of the network 10a in Fig. 1, and further description of those features already described with reference to Fig. 1 is therefore omitted.

In Fig. 2, the network 10b comprises, in addition to those elements already described above, two bitstreams B3 and B4 propagating in directions indicated by corresponding arrows and hence transferring data in opposite directions between nodes 16, 20, 22, 24, and 26 of the network.

On bitstream B3, the uppermost provided node 16 is head-end node and thus arranged to provide frame synchronization by transmitting frame start signals and guard patterns on bitstream B3. Similarly, on bitstream B4, the upstream provided node 26 is arranged to provide frame synchronization by transmitting frame start signals and guard patterns thereto.

In Fig. 2, node 16, in similar to node 18, acts as a synchronization slave node in relation to the master node 12. In this context, this means that node 16 will transmit the frame start signal on bitstream B3 in synchronization with the frame start signal received on bitstream B1 from the master node 12. Also, node 26 will act as a slave node to the slave node 16, i.e. the provision of the frame start signal on bitstream B4 will be governed by the provision of the frame start signal on bitstream B3, which in turn will be governed by the provision of the frame start signal on bitstream B1.

In the embodiment shown in Fig. 2, the node 16 is still arranged to use, e.g., one time slot per frame on bitstream B2 to transmit information, relating to the

frame synchronization situation on bitstreams B3 and B4, typically in relation to the frame rate synchronization situation on bitstreams B1 and B2, to the master node 12. This information is then received by the master node 12 and used at the master node 12 as a basis for determining how to control the provision of the trigger pattern on bitstream B1, in similar to what has already been described with reference to Fig. 1. If, for example, the information generated by node 16 and provided to the master node 12 states that, due to some reason or another, there is a difficulty in keeping the frame rate on bitstreams B3 and B4 up to speed with the frame rate on bitstreams B1 and B2, the master node 12 may decide to increase the number of time slots included in the guard band in each frame on bitstream B1, thereby increasing the length of each frame and thus decreasing the network frame rate.

The configuration of network 10c operating according to an embodiment of the invention will now be described with reference to Fig. 3. The network 10c is an expansion of the network 10b in Fig. 2, and further description of those features already described with reference to Fig. 2 is therefore omitted.

In Fig. 3, the network 10c comprises, in addition to those parts already described above, two bitstreams B5 and B6 propagating in directions indicated by corresponding arrows and hence transferring data in opposite directions between nodes 24, 30, 32, and 34.

In this example, it is assumed that node 34 is configured to act as a synchronization master node on bitstream B5. This means that node 34 is arranged to transmit the frame start signal on bitstream B5 based a clock feature that is not directly governed by a signal that has been propagated from the master node 12, such as a clock feature provided locally at node 34.

Instead, in the embodiment shown in Fig. 3, the switch node 24 is arranged to detect the frame start signal provided on bitstream B3, as well as the frame

start signal provided on bitstream B5, and to determine the occurrence of any frame drift between the two. If so, the switch node 24 will use, e.g., one time slot per frame on bitstream B6 to transmit information stating, e.g., the polarity and magnitude of any occurring frame drift to the node 34. This information is then received at node 34 as a basis for determining how to control the provision of the frame start signal on bitstream B5 in order to ensure frame synchronization consistency over the network, more specifically at the location of the switch node 24. Consequently, if, for example, a frame rate generated locally at the master node 12 differs somewhat compared to the frame rate generated locally at the node 34, this difference is compensated for by, e.g., the increasing or decreasing of the frame length on bitstream B5, for example as achieved by the increasing or decreasing of the number of guard band time slots provided by the master node 34 to each frame of the bitstream B5 or by the adjustment of a phase locked loop controlling the operation within the node 34.

As is understood, the frame drift information could just as well be transmitted from the switch node 24 to the master node 12, said master node 12 then taking care of the frame drift problem and letting the node 34 continue its operation unaffected.

The configuration of another embodiment of a network according to the invention will now be described with reference to Fig. 4. The network 10d in Fig. 4 comprises a first bitstream B9 interconnecting nodes 61, 63, 64, and 51, as well as a second bitstream B10 interconnecting nodes 61, 62, and 52, node 61 being the head-end node of both bitstreams. Moreover, the network 10d comprises a bitstream R10 interconnecting nodes 51-56 in a single ring fashion, node 51 forming both head-end and terminating-end of the bitstream.

In the network 10d, it is also assumed that node 61 is configured to act as synchronization master node for

the entire network. Node 61 will consequently define and provide the frame start signal on bitstreams B9 and B10. Node 51, while being the head-end node on the single ring bitstream R10, will be configured to provide the frame start signal on bitstream R10 as synchronized in accordance with the frame start signal received on bitstream B9 from the master node 61.

If a link or node failure were to occur on bitstream B9 in this situation, network synchronization would have to be propagated to the single ring bitstream R10 via bitstream B10 instead of via the malfunctioning bitstream B9. This would conventionally have meant that node 52 would have had to take over the role as head-end node on bitstream R10. This would very likely in turn have implied exposing all nodes attached to the bitstream R10 to a disadvantageous phase shift caused by the change of head-end, possibly resulting in loss of data.

However, using the invention, node 51 may continue to operate as head-end node during said link or node failure, while simply receiving messages from node 52 pertaining to any occurring phase drift between frames provided by node 51 on bitstream R10 and frames provided by node 61 on bitstream B10. Consequently no changing of head-end and resulting phase shifts is necessary.

The structure of a bitstream of the kind transferred on the bitstreams shown in Figs. 1-4 will now be described with reference to Fig. 5. As shown in Fig. 5, each bitstream is divided into regularly recurrent cycles or frames having an essentially fixed length, for example 125 μs. Each frame is in turn divided into fixed size, e.g. 64-bit, time slots. The number of time slots within a frame depends on the network's bit rate.

The start of each frame is defined by one or more frame synchronization slots FS transferring the frame start signal that is used to synchronize the operation of each node in relation to each frame. Also, to make sure that the number of slots in one frame will not overlap a

following frame, a guard pattern G, comprising on or more "fill" slots, is added after the last payload data slot at the end of each frame.

To be noted, in a DTM network, the remaining time slots are in general divided into two groups, control slots and data slots. The control slots are used for control signaling between nodes of the network, i.e. for carrying messages between nodes for the internal operation of the network, such as for channel establishment, slot allocation, and the like. The data slots are used for the transfer of user data (payload data) between end users connected to said nodes.

Each node will typically have access to at least one control slot and to a dynamic number of data slots within each frame of on the bitstream that is accessed by said node. Each node uses its control slot to communicate with other nodes within the network. Furthermore, the number of data slots allocated to each node may for example depend upon the transfer capacity requested by the end users served by the respective node. If the end users of a certain node require a large transfer capacity, the node will allocate more data slots for that purpose. On the other hand, if the end users of a certain node merely require a small transfer capacity, the node may limit its number of allocated data slots. The allocation of control slots and data slots to different nodes may by dynamically adjusted as the network load changes.

Figs. 6a and 6b schematically illustrates frame synchronization situations at a switch node, in this case the switch node 24 in Fig. 3, operating in relation to the two schematically shown bitstreams B3 and B5. As illustrated, each one of the bitstream comprises a stream of time slots, and each frame is defined by a frame start signal comprising one time slot (marked as a black filled square in the figures). Also, one or more guard band time slots, illustrated as hatched squares, are provided at the end of each frame.

In the situation shown in Fig. 6a, when a first frame start signal on bitstream B3 is detected by node 24, time slot number 356 is received by node 24 on bitstream B5. Then, as the next frame start signal is detected on bitstream B3, time slot number 357 is received on bitstream B5, and so on. As a result, the node 24 determines that the frame length on bitstream B3 is longer than the frame length on bitstream B5 and that the frame drift is approximately one time slot per frame. Information as to this frame drift situation is then in according to the invention transmitted, in a time slot on bitstream B6 in Fig. 3 or 4, to node 34 that controls the frame rate on bitstream B5. Based upon this information, the node 34 will add extra guard band time slots to each frame of bitstream B5 (as illustrated by the extra guard band time slot per frame of bitstream B5 in Fig. 6b), thus eliminating the frame drift.

As a result, in Fig. 6b, after this modification has taken place, at each detection of the recurrent frame start signal on bitstream B3 by the node 24, the same time slot number 360 is received by the node 24 on bitstream B5. The node 24 thus determines that there is no frame drift at the moment and preferably transmits this information to the master node.

As is understood, the configuration of the bitstreams shown in Fig. 5, 6a and 6b, for example, the number of time slots included in the synchronization patterns and the guard patterns, is merely meant to be illustrative. Hence, the size of the frame drift compared to the frame length is very exaggerated and the actual number of time slots within each frame is normally far greater than the one shown. Furthermore, the synchronization pattern need not be a single contiguous set of time slots provided at the start of each frame, but may very well be provided in other forms and configurations.

An exemplifying embodiment of a node performing the operations discussed above will now be described with

reference to Fig. 7. In Fig. 7, the node 100, which in this example is assumed to be the switch node 24 of Fig. 3, is connected to the bitstreams B3, B4 (not shown), B5 (not shown) and B6, and comprises a first bitstream access unit 102, a bit clock retrieving circuit 104, an input demultiplexor 106, an input time slot counter 108, a frame start detector 110, a second bitstream access unit 112, a switching circuit 114, and a message generator 118.

In the node 100, data, such as frame start signals, control data for network signaling, user data, guard band fill slots, and the like, are received in time slots from bitstream B3 via the bitstream access unit 102 and are supplied to the bit clock retrieving circuit 104 and the input demultiplexor 106. The bit clock retrieving circuit 104 locks the bit clock of the node to the clock rate received on bitstream B3, so that at least the input port components of the node will operate at a clock frequency corresponding to the one received on the bitstream B3. The bit clock retrieving circuit 104 provides the derived clock frequency to, among others, the input time slot counter 108. Based upon the clock frequency derived by the bit clock retrieving circuit 104, the input time slot counter 108 will count time slot positions (each time slot comprising, e.g., 64 bits), typically starting from zero to the number of time slots contained in frame.

The clock signal 109 from the input time slot counter 108 is provided to, among others, the input demultiplexor 106 and the frame start detector 110. Based upon the clock signal 109, the input demultiplexor 106 will demultiplex the input bitstream bits into 64-bit time slot data groups that are sequentially provided to, the frame start detector 110 and the switching circuit 114

The function of the frame start detector 110 is to detect the frame start signal from bitstream B3 and to reset the input time slot counter 108 based thereupon. Consequently, when detecting the frame start signal in

the data provided by the demultiplexor 106, it will output a reset signal 116 to the input time slot counter 108. Furthermore, this reset signal is also provided to the message generator 118.

In addition to the reset signal 116 from the frame start detector 110, the message generator 118 receives a similar reset signal 122 from a corresponding set of units (not shown) arranged within said node for providing access to bitstream B5. The reset signal 122 will thus provide information as to the reception of a frame start signal on bitstream B5. The message generator 118 continuously compares the timings of the reception of the reset signal 116 from the detector 110 and the timings of the reception of the reset 122 signal. As an output, the message generator 120 generates time slot data that provide information as the occurrence of any frame drift between the frame start signals of bitstream B3 and B5 (or the occurrence of, for example, a link or node failure). This data is then transmitted, using the bitstream access unit 112, to a synchronization providing node typically attached to the bitstream B6.

Generally, the bitstream access unit 112 will generate a frame start signal to be provided to bitstream B6 either using the reset signal from the detector 110 or using a locally generated clock signal (not shown) as reference. Typically, the bitstream access unit 112 may use the reset signal 116 as a reference when acting as an intermediate node or as a synchronization slave node, but may use a locally generated clock signal (not shown) as a reference when acting as a synchronization master node.

In the latter case, i.e. when acting as a "head end" or frame synchronization providing node, in Fig. 7, the bitstream access unit 112 is provided to receive data relating to frame drift or the like from bitstream B3 via the input demultiplexor 106. Hence, the bitstream access unit 112 is then provided to adjust the transmission of

the frame start signal on bitstream B6 in consideration of any frame drift data received from bitstream B3.

Hence, the functions provided by a) the frame synchronization monitoring message generator 118 and b) the frame drift message receiving bitstream access unit 112 basically embody two different aspects of the invention.

As understood, the node 100 in Fig. 7 is typically arranged to switch data according to currently established channels. However, with the exemption of the schematically illustrated switching circuit 114, dedicated means for performing and controlling the actual switching of data in space and time are not shown in Fig. 7.

Although exemplifying embodiments of the invention have been described in detail above with reference to the accompanying drawings, the invention is of course not limited thereto. Consequently, as is understood by those skilled in the art, modifications, alterations, and combinations thereof will fall within scope of the invention, as defined by the accompanying claims.